**Lab 3 Report**

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Group 8

**Design Questions**

***1. What is the minimum required DAC sample rate to achieve the frequency output requirements? Hint: look up the Nyquist Sampling Theorem.***

According to the Nyquist Sampling Theorem, the sample rate should be twice whatever frequency you are sampling. In our case,

***2. At the DAC's maximum serial clock frequency, what is the maximum single-channel sample rate using the write-and-update command while still meeting the delay-after-update requirement? Reference which parameters in the datasheet are needed to determine this specification. Hint: determine the data period first.***

The maximum sample rate should be about 500kHz, since shifted data bits period is 32 \* 1/50\*106 s, which is insignificant compared to the minimum sync high time 2 µs.

***3. What sample rate does your design use? How does this affect the appearance of the DAC output at higher frequencies?***

Our sample rate is ~217kHz. At higher frequencies, we do observe discrete non smooth behavior of the sine wave if we zoom in enough.

***4. What are the GPIO signals used to connect to the pins of the DAC interface? Use the expansion board schematic and the GPIO documentation page on Blackboard.***

The GPIO signals used for DAC are:

GPIO\_0[10] = ~SYNC;

GPIO\_0[8] = SCLK;

GPIO\_0[9] = Din;

GPIO\_0[11] = ~LDAC;

GPIO\_0[12] = ~CLR;

***5. For your mono-channel output, which DAC command does your design use?***

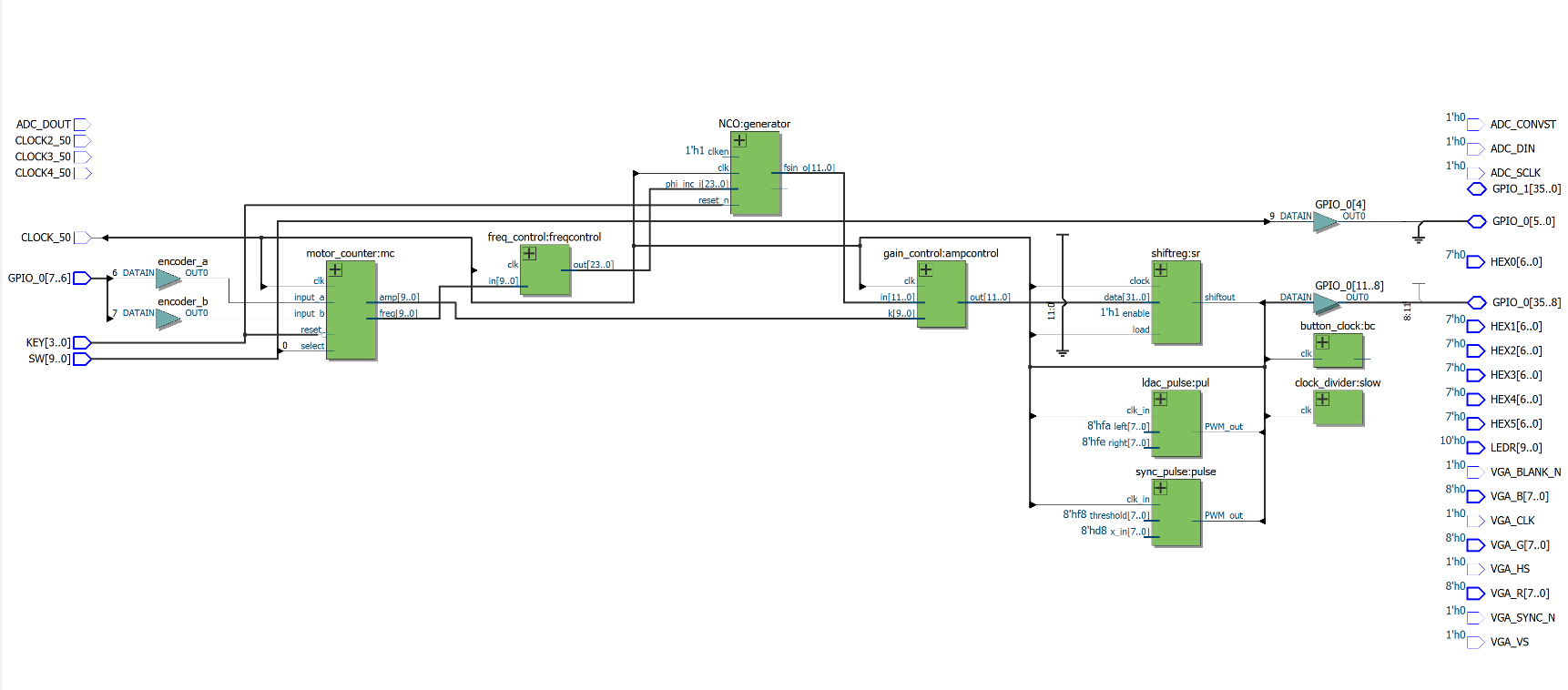
We use 0011 for our command bits, which is write and update the DAC channel

***6. How do you control the NCO such that each sample is sent to the DAC correctly?***

We use 12 bit of magnitude resolution so that it fits exactly with DAC’s data bits, then assigning them to specific 12 bits in the data packets that also contain command and address in front of the data.

***7. Find the equation in the NCO datasheet that shows how to calculate sine frequency versus phase increment. Since your sample rate is the effective clock rate of the NCO, what range of phase increments do you need to meet the output frequency specification?***

F(output\_of\_sinusoid) = [Phase\_increment/(2N)] \* F(clk) where:t F(output\_of\_sinusoid) = Desired output frequency of the NCO Compiler, N = Accumulator bit width, and F(clk) = Input clock frequency

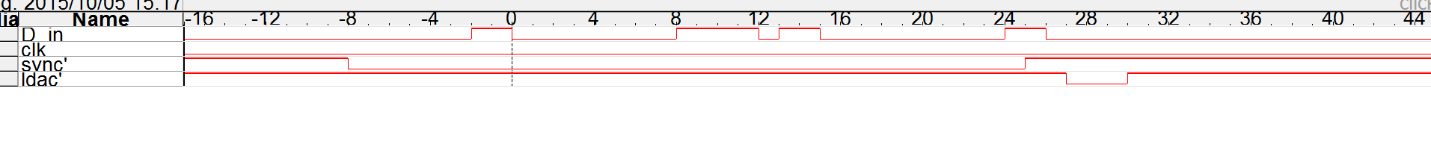
****Design Diagram and Module Functionality**

***Block diagrams:***

***LPM\_SHIFTREG IP:***

We required the shiftreg to shift left, and take only parallel input to produce only serial data output, also a clock enable is implemented. No additional inputs were added.

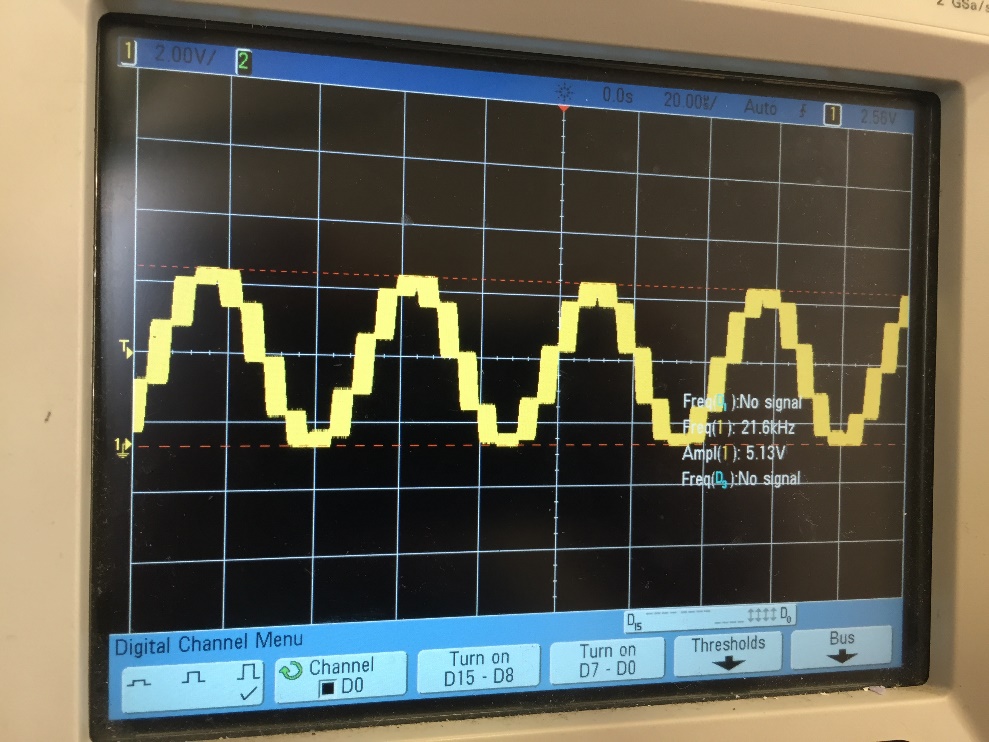
***DAC signaltap:***

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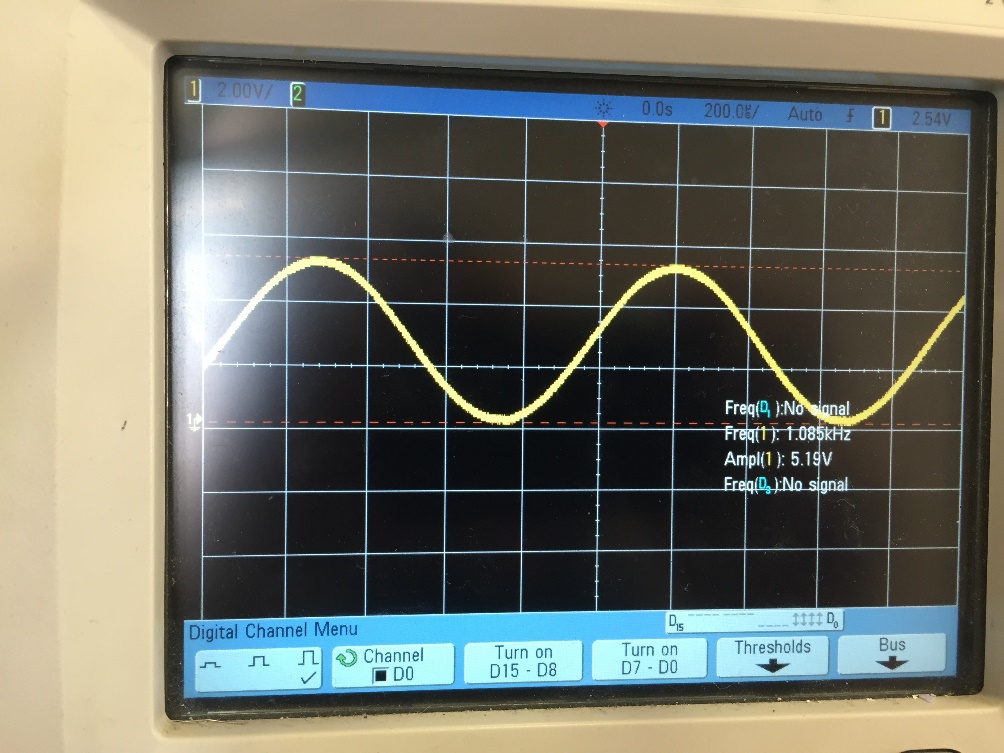
clk is not displayed due to signal tap uses CLOCK\_50 for its clk.

**Oscilloscope Captures**

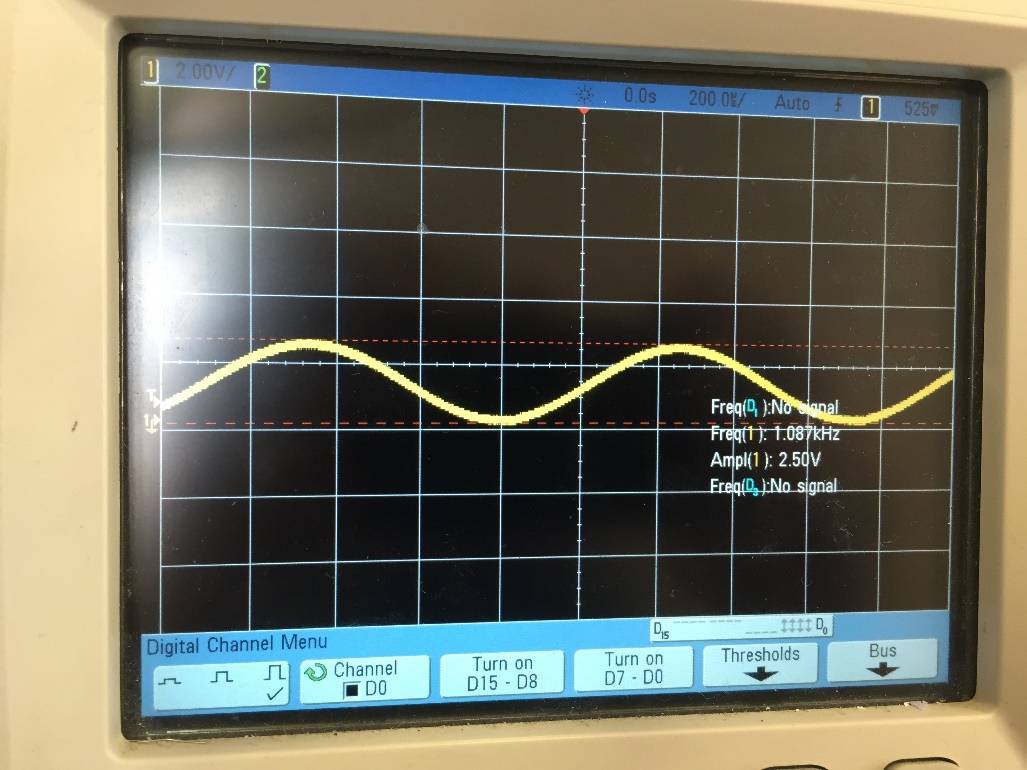
Max frequency, max amplitude

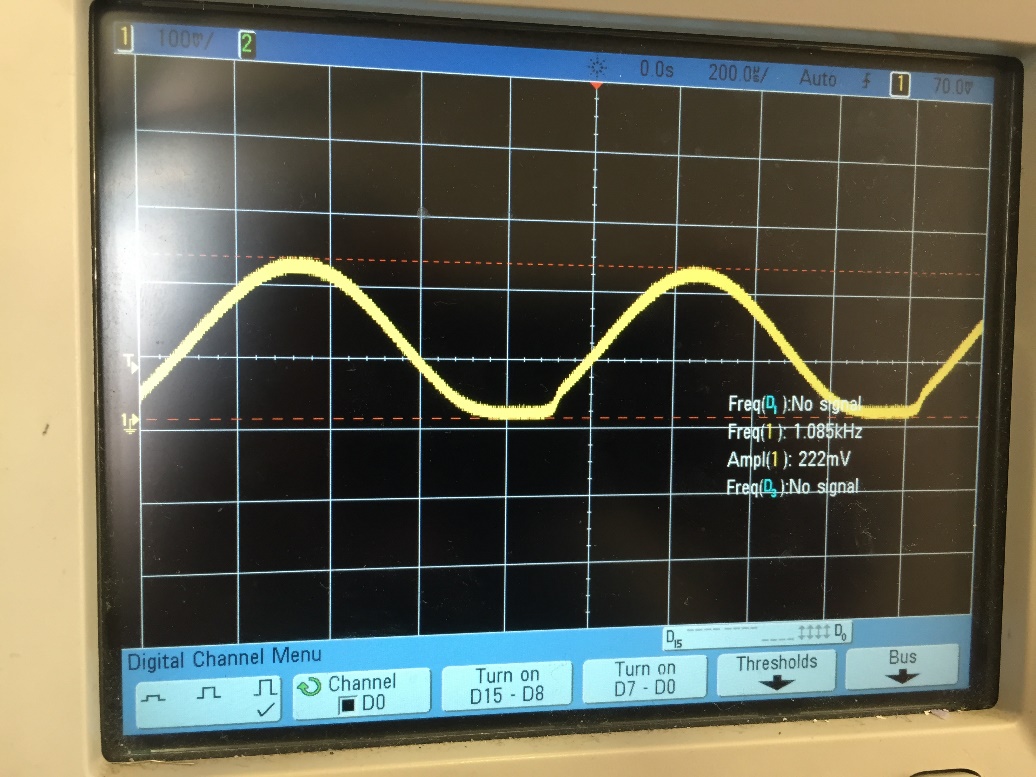
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Default frequency, max amplitude

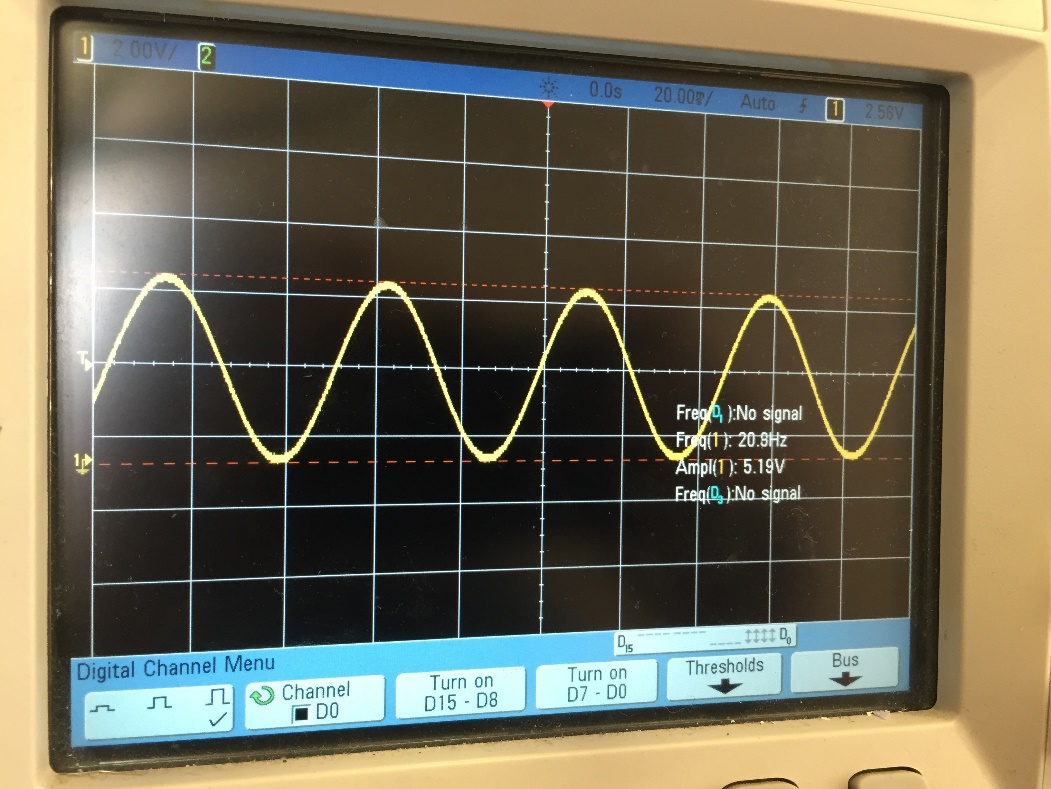
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Default frequency, half amplitude

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****Default frequency, 5% amplitude

Minimum frequency, max amplitude

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**Collaboration**

We write draft codes and using github to exchange, working in lab together to debug.