**Lab 2 Report**

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Group 8

**Design Questions**

***1. What is the minimum required DAC sample rate to achieve the frequency output requirements? Hint: look up the Nyquist Sampling Theorem.***

According to the Nyquist Sampling Theorem, the sample rate should be twice whatever frequency you are sampling. In our case,

***2. At the DAC's maximum serial clock frequency, what is the maximum single-channel sample rate using the write-and-update command while still meeting the delay-after-update requirement? Reference which parameters in the datasheet are needed to determine this specification. Hint: determine the data period first.***

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***3. What sample rate does your design use? How does this affect the appearance of the DAC output at higher frequencies?***

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***4. What are the GPIO signals used to connect to the pins of the DAC interface? Use the expansion board schematic and the GPIO documentation page on Blackboard.***

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***5. For your mono-channel output, which DAC command does your design use?***

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***6. How do you control the NCO such that each sample is sent to the DAC correctly?***

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***7. Find the equation in the NCO datasheet that shows how to calculate sine frequency versus phase increment. Since your sample rate is the effective clock rate of the NCO, what range of phase increments do you need to meet the output frequency specification?***

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**Code Organization**

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**Design Diagram and Module Functionality**

**Oscilloscope Captures**

**Collaboration**

We write draft codes and using github to exchange, working in lab together to debug.